CLAIMS

What is claimed is:

1. A flash memory cell comprising:

a substrate having a source region, a drain region, and a channel region coupled between said source region and said drain region;

a floating gate, having a charge trapping region and a first fin region, wherein said charge trapping region is coupled to said channel region and said fin region is coupled to said source region;

a control gate coupled to said charge trapping region.

2. The flash memory cell according to Claim 1, wherein said first fin region reduces drain to source leakage current.

3. The flash memory cell according to Claim 1, wherein said first fin region increases drain to source read current.

4. The flash memory cell according to Claim 1, wherein said first fin region reduces drain induced barrier reduction.

5. The flash memory cell according to Claim 1, wherein said first fin region reduces barrier scattering.

6. The flash memory cell according to Claim 1, wherein said floating gate further comprises a second fin region, wherein said second fin region is coupled to said drain region.

7. The flash memory cell according to Claim 6, wherein said second fin region reduces drain to source leakage current.

8. The flash memory cell according to Claim 6, wherein said second fin region increases drain to source read current.

9. A method of manufacturing a floating gate transistor comprising:

forming a first insulating layer on a substrate;

forming a floating gate on said first insulating layer;

forming a second insulating layer on said floating gate;

forming a control gate on said second insulating layer;

doping a portion of said floating gate, wherein a fin region is formed; and

doping a source region and a drain region in said substrate proximate respective first end and second end of said floating gate having said fin.

10. The method according to Claim 9, wherein said forming said floating gate comprises:

depositing a first semiconductor layer on said first insulating layer; and

patterning said first semiconductor layer utilizing photolithography and selective etching.

11. The method according to Claim 9, wherein said forming said control gate comprises:

depositing a second semiconductor layer on said second insulating layer; and

patterning said second semiconductor layer utilizing photolithography and selective etching.

12. The method according to Claim 9, wherein:

said doping said portion of said floating gate comprises implanting acceptor impurities; and

said doping said source region and a drain region comprises implanting donor impurities.

13. The method according to Claim 9, wherein said fin region overlaps said source region.

14. A floating gate transistor comprising:

a source;

a drain;

a channel disposed between said source and said drain;

a charge trapping region disposed above said channel region;

a first fin disposed adjacent said charge trapping region and above said source;

a first isolation layer disposed above said channel and said source and below said charge trapping region and said first fin;

a control gate disposed above said charge trapping region; and

a second isolation layer disposed above said charge trapping region and said first fin and below said control gate.

15. The floating gate transistor according to Claim 14, wherein said first fin comprises p-doped semiconductor.

16. The floating gate transistor according to Claim 14, further comprising:

a second fin disposed adjacent said charge trapping region and above said drain; and

said first isolation layer further disposed above said drain and below said second fin.

17. The floating gate transistor according to Claim 16, wherein said second fin comprises p-doped semiconductor.

18. The floating gate transistor according to Claim 14, wherein:

said source comprises n-doped semiconductor;

said drain comprises n-doped semiconductor; and

said channel comprises p-doped semiconductor.

19. The floating gate transistor according to Claim 14, wherein:

said source comprises p-doped semiconductor;

said drain comprises p-doped semiconductor; and

said channel comprises n-doped semiconductor.

20. The floating gate transistor according to Claim 14, wherein:

said first insulating layer comprises a dielectric; and

said second insulating layer comprises a dielectric.